

FIG. 1

22 or 26

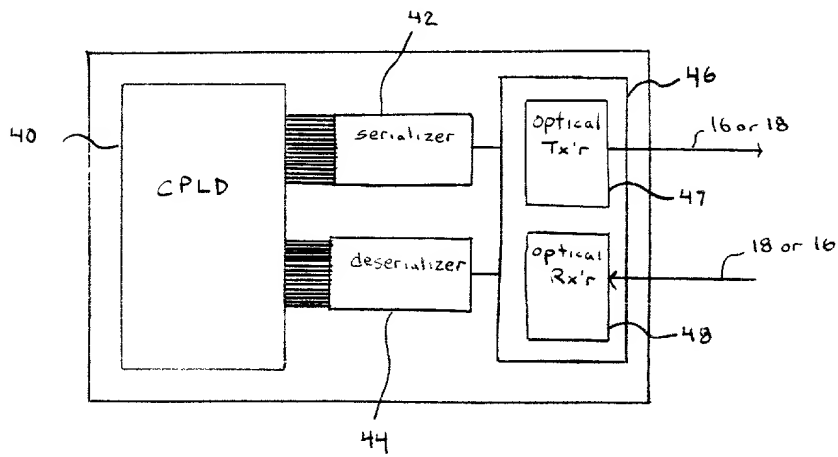


FIG. 2

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Data	Signals ^a	Bit	Data Rate	Comments
<i>up to RF Equipment</i>				
Tx Data Bus	LTXO1A10	0	19 6608 MHz	Each sector muxed at 78 6432 MHz
	LTXO1A11	1	19 6608 MHz	
	LTXO1AQ0	2	19 6608 MHz	
	LTXO1AQ1	3	19 6608 MHz	
ARCNET Bus	ARCNET_TXEN	10, 11	1 25 Mbps	
Even Second Tick	EVEN_SEC	12 (Transmitted on one multiplexed channel)	19 6608 MHz	1 pulse every 2 sec, 19.6608 MHz resolution
Radio serial port	CBRSER		Low	To PCBR
Serial port from Radio Controller	CRCSER		Low	Reserved for future use
Radio RF Emergency Switch	CBR_SW		Static	To PCBRs, one to PCBR in each RFU
CCU Available	CAVAIL_N		static	static, transmit in control channel One to each of three RFUs
Spare	-		-	
Spare	-		-	
Physical Address	RF Enclosure_ID (3 0)	13 (Transmitted on one multiplexed channel)	static	4 unique bits to each RFU
Multiplex Sync Pulse		14	2 4576 Mbps	
Spare		4	-	Reserved for future use
Spare		5	-	Reserved for future use
Spare		6	-	Reserved for future use
Spare		7	-	Reserved for future use
Spare	-	8	-	Reserved for future use
Spare	-	9	-	Reserved for future use
Parity	-	15	-	Parity check
19.6608 MHz clock			Not Sent; SCLK23 clock is recovered in RF Enclosure, SCLK34 is then generated from SCLK23	

FIG. 3

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slot/bit	0	1	2	3	4	5	6	7	8	9
data	LTXO1A10	LTXO1A11	LTXO1AQ0	LTXO1AQ1	Spare	Spare	Spare	Spare	Spare	Spare
slot/bit	10	11	12	13	14	15	16	17	18	19
data	ARCNET_EN	ARCNET	Mux	Mux	Mux Sync	Parity	Reserved for FOM Use			

FIG. 4

Data	Signals ^a	Bit	Data Rate	Comments
<i>down to BBU</i>				
RXDATA	RXIA0	0	19 6608 MHz	div0/div1 are multiplexed in data stream
	RXIA1	1	19 6608 MHz	
	RXIA2	2	19 6608 MHz	
	RXIA3	3	19 6608 MHz	
	RXQA0	4	19 6608 MHz	
	RXQA1	5	19 6608 MHz	
	RXQA2	6	19 6608 MHz	
	RXQA3	7	19 6608 MHz	
ARCNET	ARCNET_RX	11	1 25 Mbps	
Bypass from radio	CLBYP_N	12 (one muxed channel)	Static	From radio
Serial Port to CDMA Radio Controller	CRCSER		low	
Radio Serial Port	CBRSER		low	
Spare	-		-	reserved for future use
Spare	-		-	reserved for future use
Spare	-		-	reserved for future use
Spare	-		-	reserved for future use
Spare	-		-	reserved for future use
Demultiplexer Sync		14	2 4576 Mbps	
Parity	-	15	-	Parity check
Spare	-	8	-	reserved for future use
Spare	-	9	-	reserved for future use
Spare	-	10	-	reserved for future use
Spare	-	13	-	reserved for future use

Fig. 5

slot/bit	0	1	2	3	4	5	6	7	8	9
data	RXIA0	RXIA1	RXIA2	RXIA3	RXQA0	RXQA1	RXQA2	RXQA3	Spare	Spare
slot/bit	10	11	12	13	14	15	16	17	18	19
data	Spare	ARCNET	Mux	Spare	Mux Sync	Parity	Reserved for FOM use			

Fig. 6